Due in class, Tuesday, 11 October.

Problem 1

The input to a particular electrical device can be modeled as a 10-kΩ resistance in parallel with a 100-nF capacitance. At $t = 0$, a 5-V source with 2-kΩ Thevenin resistance is suddenly connected to the electrical device. Determine the voltage at the input to the device as a function of time, and indicate the time needed for this voltage to rise to 50% of its final value. Assume zero voltage for $t < 0$.

Problem 2

The capacitor is uncharged for $t < 0$. Switch A closes at $t = 0$. Then switch A opens and switch B closes at $t = 3$ ms. Determine $i_x$ at $t = 10$ ms.
Problem 3

The switch closes at $t = 0$, having been open for a long time. Find $v_x(t)$. 

Problem 4

Design a circuit that controls windshield wipers. The circuit must produce a 5-V pulse of 1-s duration at 2-s, 4-s, or variable 6- to 10-s intervals. Assume that the 5-V pulse interacts with other ciruity to move the wipers through one cycle. See the attached notes pertaining to the 555 timer.

Problem 5

The switch opens at $t = 0$, having been closed for a long time. Find $i_x(t)$. 
1.3 Mixed-Signal Systems: The 555 Timer

Analog or digital? The 555 Timer has been around since the early 1970s. And even with the occasional new arrival of challengers offering improved performance, it remains a low-cost integrated circuit with popular appeal. Analog and digital signals will increasingly play co-operative and equally important roles as complex mixed-signal systems evolve.

In relation to the black box shown in Fig. 1.31, the 555 timer sports:

- Two power connections — \( V^+ \) (pin 8) and ground (pin 1).
- Two inputs — The trigger (pin 2) and threshold (pin 6) are inputs that only have effect when they are made less than or greater than specific reference voltages.
- Two outputs — The output (pin 3) and discharge (pin 7) assume one of two states: When the output is HIGH (typically \( V^+ - 0.9 \) V), the discharge connection appears as an open circuit. When the output is LOW (typically 0.2 V), the discharge connection appears as a short circuit to ground.
- Two special connections — The reset (pin 4) forces a LOW output at pin 3 when set to a LOW voltage, and it has no effect when set to a HIGH voltage. The control (pin 5) is used to change the values of the reference voltages that govern the behavior of the two inputs. (We shall tend to ignore both special connections.)

Figure 1.31: Pin designations for the 555 timer.

There are three simple governing rules:

**Rule 1:** Barring a conflict with Rule 2, the output goes HIGH and stays there if the trigger voltage is made less than \((1/3)V^+\).

**Rule 2:** Barring a conflict with of Rule 1, the output goes LOW and stays there if the threshold voltage is made greater than \((2/3)V^+\).

**Rule 3:** The input terminal currents are ideally zero.
Monostable Behavior

What do the 555-timer rules imply? Suppose the initial output, trigger, and threshold voltages are LOW, 6 V, and 0 V, respectively, and let \( V^+ = 6 \) V. If the trigger is subsequently set to 0 V, which is less than \((1/3)V^+ = 2 \) V, Rule 1 tells us that the output will become HIGH and stay there indefinitely (even as the trigger is set back to 6 V shortly afterwards). This is consistent with the trigger and output waveforms shown in Fig. 1.32.

![Figure 1.32: 555 trigger and output waveforms.](image)

Nothing very exciting so far. However, we can limit the time duration of the HIGH output condition by taking advantage of Rule 2—we merely force the threshold voltage above \((2/3)V^+ = 4 \) V at a desired time following the completion of the trigger pulse. One way to do this is to connect the threshold input to the \( RC \) circuit shown in Fig. 1.33a. The initial threshold voltage \( v_{th} \) is 0 V, and the threshold terminal draws no current (Rule 3). Thus, at time \( t \),

\[
v_{th} = V^+ \left(1 - e^{-t/RC}\right). \tag{1.29}
\]

In turn, \( v_{th} = (2/3)V^+ \) at time

\[
T = RC \ln 3 = 1.1 RC. \tag{1.30}
\]

The consistent threshold and output waveforms appear in Fig. 1.33b.

![Figure 1.33: (a) 555 threshold circuit; (b) threshold and output waveforms.](image)
Things are looking much better, apart from a minor technical difficulty: How can we ensure that the threshold voltage begins to rise when the 555 output goes HIGH? And how can we ensure that the system produces another output pulse in response to a subsequent trigger signal?

Both problems resolve by tying the 555 discharge to the threshold input. When the output is initially LOW, the discharge appears as a short circuit to ground, and it holds the threshold voltage to an approximate zero level. When the output becomes HIGH, the discharge appears as an open circuit, and the threshold voltage is made free to rise. When the output becomes LOW again, the discharge forces the threshold voltage back near zero.

So now we have a 555 monostable or one-shot circuit that produces a long output pulse of fixed duration in response to a shorter trigger pulse of arbitrary duration. Figure 1.34 shows the complete monostable circuit. Note that the reset terminal is tied to \( V^+ \), and the control terminal is tied to ground through a 0.01-µF capacitor (to suppress undesired transients).

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**Exercise 1.8** A 555 monostable circuit is intended to produce a 0.5-s output pulse subject to a design with \( C = 0.1 \) µF. Determine \( R \).

**Ans:** \( R = 4.5 \) MΩ

**Exercise 1.9** The capacitor of the preceding exercise discharges through an effective resistance of 1 Ω. Determine the time needed for the threshold voltage to return to 0.2 V from its highest value. Assume \( V^+ = 6 \) V.

**Ans:** \( t = 0.3 \) µs

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Astable Behavior

The prospects for another useful 555 circuit will soon become apparent with the help of Fig. 1.35. Here, voltage $v_c$ is $(2/3)V^+$ when the switch is closed at $t = 0$. Our interest is the time at which $v_c = (1/3)V^+$.

![Figure 1.35: RC demonstration circuit.](image)

The capacitor voltage decreases exponentially between initial and final values with time constant $R_1C$. Specifically,

$$v_c(t) = v_{\text{final}} + (v_{\text{initial}} - v_{\text{final}}) e^{-t/R_1C}.$$  \hspace{1cm} (1.31)

So with $v_{\text{initial}} = (2/3)V^+$ and $v_{\text{final}} = 0$,

$$v_c(t) = \frac{2}{3} V^+ e^{-t/R_1C}.$$  \hspace{1cm} (1.32)

And when $v_c = (1/3)V^+$,

$$t = t_1 = R_1C \ln 2 = 0.693 R_1C.$$  \hspace{1cm} (1.33)

Now open the switch again at $t' = t - t_1 = 0$. Our new interest is the time at which $v_c = (2/3)V^+$, the initial condition for the preceding process. The capacitor voltage increases exponentially between $v_{\text{initial}} = (1/3)V^+$ and $v_{\text{final}} = V^+$ with time constant $(R_1 + R_2)C$. Thus, we look to the form of Eq. 1.31 to obtain

$$v_c(t') = V^+ - \frac{2}{3} V^+ e^{-t'/(R_1+R_2)C}.$$  \hspace{1cm} (1.34)

In turn, when $v_c = (2/3)V^+$,

$$t' = t_2 = (R_1 + R_2)C \ln 2 = 0.693 (R_1 + R_2)C.$$  \hspace{1cm} (1.35)

If the switching cycle repeats indefinitely, the frequency is

$$f = \frac{1}{t_1 + t_2} = \frac{1.443}{(2R_1 + R_2)C}.$$  \hspace{1cm} (1.36)
Enter the 555 timer. In consideration of Rule 1 and Rule 2, we connect the trigger and threshold inputs to \( v_c \) so that the 555 output becomes HIGH when \( v_c < (1/3)V^+ \) and LOW when \( v_c > (2/3)V^+ \). The \( v_c \) time dependence is not affected (Rule 3). Thus, the LOW and HIGH intervals are \( t_1 \) and \( t_2 \), respectively.

While the 555 output is LOW (and \( v_c \) decreases), the discharge appears as a short circuit to ground—just like the switch. And while the 555 output is HIGH (and \( v_c \) increases), the discharge appears as an open circuit—just like the switch. So we can eliminate the switch and, more importantly, sustain the switching cycle by connecting the discharge to the node between \( R_1 \) and \( R_2 \). Here is yet another triumph for circuit feedback.

Figure 1.36 shows the complete **astable** circuit.

![555 astable circuit](image)

Figure 1.36: 555 astable circuit.

The **duty cycle** of the pulse train produced by a 555 astable circuit is defined as the ratio of the HIGH interval \( (t_2) \) to the waveform period \( (t_1 + t_2) \). Thus, in consideration of Eqs. 1.33 and 1.35,

\[
\text{duty cycle} = \frac{R_1 + R_2}{2R_1 + R_2} \times 100 \%.
\]  

Exercise 1.10  A 555 astable circuit with the form of Fig. 1.36 is intended to produce a 2-kHz pulse train with 80% duty cycle subject to a design with \( C = 0.1 \mu\text{F} \). Determine \( R_1 \) and \( R_2 \).

**Ans:**  \( R_1 = 1.4 \text{ k}\Omega, R_2 = 4.4 \text{ k}\Omega \)
Inside the 555 Black Box

Peel back the cover of a 555 timer, and you will see the assortment of interconnected components and black boxes shown in Fig. 1.37. Abstractly, you find a chain of three equal-value resistors between $V^+$ and ground, two op-amp-like comparators, an $RS$ latch, and an electronic device called a transistor—actually an npn bipolar junction transistor or BJT. No doubt you have heard of this last component, as it pervades the popular culture. For the moment, we treat the BJT as an especially fundamental black box that functions like a switch: there is an effective short circuit between the C (collector) and E (emitter) terminals when the B (base) terminal is tied through a resistor to a HIGH voltage level, and there is an open circuit between C and E when B is similarly connected to a LOW voltage level. In practice, the BJT rules are much more complicated.

![Figure 1.37: Inside the 555 timer.](image)

The new 555 abstraction explains the output and discharge conditions encountered previously. When the external output is HIGH, the internal $Q$ output of the $RS$ latch is also HIGH, and its complement $\bar{Q}$ is LOW, which induces the BJT to make the discharge appear as an open circuit. But when the external output is LOW, $Q$ and $\bar{Q}$ are LOW and HIGH, respectively, and the latter induces the BJT to make the discharge appear as a short circuit to ground.

Meanwhile, the internal comparators draw zero input currents (Rule 3). The three-resistor voltage divider is thus made free to establish reference voltages of $(2/3)V^+$ at node A and $(1/3)V^+$ at node B (provided that there is an open connection at the external control terminal). Then we have . . .
• **Rule 1:** Barring a conflict with Rule 2 means that the threshold voltage is less than \((2/3)V^+\) so that comparator 1 yields a LOW voltage at the \(R\) input to the latch. And when the trigger voltage becomes less than \((1/3)V^+\), comparator 2 yields a HIGH voltage at the \(S\) input to the latch. In turn, \(Q\) is “set” HIGH.

• **Rule 2:** Barring a conflict with Rule 1 means that the trigger voltage is greater than \((1/3)V^+\) so that comparator 2 yields a LOW voltage at the \(S\) input to the latch. And when the threshold voltage becomes greater than \((2/3)V^+\), comparator 1 yields a HIGH voltage at the \(R\) input to the latch. In turn, \(Q\) is “reset” LOW.

... as advertised.

Engineers design *with* integrated circuits—
only a relatively few design integrated circuits.

But woe to the engineer who overlooks the specifics of black-box interiors (see Problem 1.91).

→ Peel back the cover of an op-amp or comparator, and you will see an assortment of interconnected transistors that function much like valves—they pass current, but in an intermediate sense with not just all or nothing. How do they establish a large (but not infinite) differential voltage gain? What factors contribute to input offset voltage?

→ Peel back the cover of an RS flip-flop and the several covers of the gates within it, and you will see an assortment of interconnected transistors that function much like switches—shorted when closed, no current when open. How do they recognize and establish particular HIGH and LOW levels? What time constraints apply?

→ Peel back the cover of a (black-box) transistor, and you will find a device structure that is governed by a coterie of material and physical principles. What is the best transistor for valve- or switch-like applications?

Electronics is a discipline with an endless hierarchy of little black boxes. All of these boxes function with individual sets of ideal rules. Nevertheless, it is necessary to ask

*When do the ideal black-box rules break down?*

Alas, you probably skipped right over the Preface—just like most readers. So it bears repeating that this text concerns the fragility of black-box rules. Try as we may to understand electronics at the highest levels of abstraction, there’s no escaping the need to peel back the covers. We are poised to begin by acquiring some fundamental electronic concepts in Chapters 2 - 8.